In the Specification

Please replace the paragraph beginning at page 4, line 13, with the following rewritten paragraph:

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Fig. 1 illustrates an exemplary 1x1 ManArray two context core operable in a first context as a 1x1 and in a second context as a 1x0 SP ManArray iVLIW processor in accordance with the present invention;

Fig. 2 provides a high-level view of the basic function of the S/P-bit and context switch bit (CSB) for improved context switch control in accordance with the present invention;

Fig. 3 specifies the logical operation of various array configurations for different settings of the CSB and the instruction's S/P-bit;

Fig. 4 illustrates an exemplary 1x2 two context ManArray processor configurable as a 1x2 in context-0 and as a 1x1 in context-1; and

Figs. 5A and 5B illustrate ~~illustrates~~ an exemplary 1x5 two context ManArray processor configurable as a 1x5 in context-0 and as a 2x2 in context-1.

Please replace the paragraph beginning at page 5, line 2, with the following rewritten paragraph:

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Further details of a presently preferred ManArray core, architecture, and instructions for use in conjunction with the present invention are found in U.S. Patent Application Serial No. 08/885,310 filed June 30, 1997, now U.S. Patent No. 6,023,753, U.S. Patent Application Serial No. 08/949,122 filed October 10, 1997, U.S. Patent Application Serial No. 09/169,255 filed October 9, 1998, U.S. Patent Application Serial No. 09/169,256 filed October 9, 1998, U.S. Patent Application Serial

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No. 09/187,539 filed November 6, 1998, U.S. Patent Application Serial No. 09/205,558 filed December 4, 1998, U.S. Patent Application Serial No. 09/215,081 filed December 18, 1998, U.S. Patent Application Serial No. 09/228,374 filed January 12, 1999 and entitled "Methods and Apparatus to Dynamically Reconfigure the Instruction Pipeline of an Indirect Very Long Instruction Word Scalable Processor", U.S. Patent Application Serial No. 09/238,446 filed January 28, 1999, U.S. Patent Application Serial No. 09/267,570 filed March 12, 1999, U.S. Patent Application Serial No. 09/337,839 filed June 22, 1999, U.S. Patent Application Serial No. 09/350,191 filed July 9, 1999, U.S. Patent Application Serial No. 09/422,015 filed October 21, 1999 entitled "Methods and Apparatus for Abbreviated Instruction and Configurable Processor Architecture", U.S. Patent Application Serial No. 09/432,705 filed November 2, 1999 entitled "Methods and Apparatus for Improved Motion Estimation for Video Encoding", U.S. Patent Application Serial No. 09/471,217 filed December 23, 1999 entitled "Methods and Apparatus for Providing Data Transfer Control", U.S. Patent Application Serial No. 09/472,372 filed December 23, 1999 entitled "Methods and Apparatus for Providing Direct Memory Access Control", U.S. Patent Application Serial No. [[_____]] 09/596,103 entitled "Methods and Apparatus for Data Dependent Address Operations and Efficient Variable Length Code Decoding in a VLIW Processor" filed June 16, 2000, U.S. Patent Application Serial No. [[_____]] 09/598,566 entitled "Methods and Apparatus for Generalized Event Detection and Action Specification in a Processor" filed June 21, 2000, U.S. Patent Application Serial No. [[_____]] 09/598,564 entitled "Methods and Apparatus for Initiating and Resynchronizing Multi-Cycle SIMD Instructions" filed June 21, 2000, U.S. Patent Application Serial No. [[_____]] 09/598,558 entitled "Methods and Apparatus for Providing Manifold Array (ManArray) Program Context Switch with Array Reconfiguration Control" filed June 21, 2000, and U.S. Patent Application

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Serial No. [[_____]] 09/598,084 entitled "Methods and Apparatus for Establishing Port Priority Functions in a VLIW Processor" filed June 21, 2000, as well as, Provisional Application Serial No. 60/113,637 entitled "Methods and Apparatus for Providing Direct Memory Access (DMA) Engine" filed December 23, 1998, Provisional Application Serial No. 60/113,555 entitled "Methods and Apparatus Providing Transfer Control" filed December 23, 1998, Provisional Application Serial No. 60/139,946 entitled "Methods and Apparatus for Data Dependent Address Operations and Efficient Variable Length Code Decoding in a VLIW Processor" filed June 18, 1999, Provisional Application Serial No. 60/140,245 entitled "Methods and Apparatus for Generalized Event Detection and Action Specification in a Processor" filed June 21, 1999, Provisional Application Serial No. 60/140,163 entitled "Methods and Apparatus for Improved Efficiency in Pipeline Simulation and Emulation" filed June 21, 1999, Provisional Application Serial No. 60/140,162 entitled "Methods and Apparatus for Initiating and Re-Synchronizing Multi-Cycle SIMD Instructions" filed June 21, 1999, Provisional Application Serial No. 60/140,244 entitled "Methods and Apparatus for Providing One-By-One Manifold Array (1x1 ManArray) Program Context Control" filed June 21, 1999, Provisional Application Serial No. 60/140,325 entitled "Methods and Apparatus for Establishing Port Priority Function in a VLIW Processor" filed June 21, 1999, Provisional Application Serial No. 60/140,425 entitled "Methods and Apparatus for Parallel Processing Utilizing a Manifold Array (ManArray) Architecture and Instruction Syntax" filed June 22, 1999, Provisional Application Serial No. 60/165,337 entitled "Efficient Cosine Transform Implementations on the ManArray Architecture" filed November 12, 1999, and Provisional Application Serial No. 60/171,911 entitled "Methods and Apparatus for DMA Loading of Very Long Instruction Word Memory" filed December 23, 1999, Provisional Application Serial No. 60/184,668 entitled "Methods and Apparatus for Providing

A2 Bit-Reversal and Multicast Functions Utilizing DMA Controller" filed February 24, 2000, Provisional Application Serial No. 60/184,529 entitled "Methods and Apparatus for Scalable Array Processor Interrupt Detection and Response" filed February 24, 2000, Provisional Application Serial No. 60/184,560 entitled "Methods and Apparatus for Flexible Strength Coprocessing Interface" filed February 24, 2000, and Provisional Application Serial No. 60/203,629 entitled "Methods and Apparatus for Power Control in a Scalable Array of Processor Elements" filed May 12, 2000, respectively, all of which are assigned to the assignee of the present invention and incorporated by reference herein in their entirety.

Please replace the paragraph beginning at page 8, line 5, with the following rewritten paragraph:

A3 Sub B2 In this exemplary system 100, common elements are used throughout to simplify the explanation, though actual implementations are not so limited. For example, the execution units 131 in the combined SP/PE0 101 can be separated into a set of execution units optimized for the control function, e.g. fixed point execution units, and the PE0 as well as any other PE that could be attached can be optimized for a floating point application. For the purposes of this description, it is assumed that the execution units 131 are of the same type in the SP/PE0 and in the additional PE or PEs, such as PE1 of Fig. 4 or PEs 1, 2 or 3 of Fig. 5. In a similar manner, SP/PE0 and the other PEs ~~PE/PEs~~ use a five instruction slot iVLIW architecture which contains a very long instruction word memory (VIM) memory 109 and an instruction decode and VIM controller function unit 107 which receives instructions as dispatched from the SP/PE0's I-Fetch unit 103 and generates the VIM addresses-and-control signals 108 required to access the iVLIWs stored in the VIM. These iVLIWs are identified by the letters SLAMD in VIM 109. The loading

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of the iVLIWs is described in further detail in U.S. Patent Application Serial No. 09/187,539 entitled "Methods and Apparatus for Efficient Synchronous MIMD Operations with iVLIW PE-to-PE Communication". Also contained in the SP/PE0 is [[a]] an SP reconfigurable register file 111 and a PE reconfigurable register file 127 which is described in further detail in U.S. Patent Application Serial No. 09/169,255 entitled "Methods and Apparatus for Dynamic Instruction Controlled Reconfiguration Register File with Extended Precision".

Please delete the paragraph beginning at page 9, line 16, as shown:

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~~All of the above noted patent applications are assigned to the assignee of the present invention and incorporated herein by reference in their entirety.~~

Please replace the paragraph beginning at page 13, line 7, with the following rewritten paragraph:

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To further support the context switch mechanism and provide support for multiple contexts, an additional mechanism is added to allow one of the register files to be saved and restored from memory in the background while a task is using another register file referred to as the foreground register file. One mechanism used for this takes advantage of unused load and store unit instruction slots to perform this context switch save and restore operation. Essentially, "background" store and load instructions, together with a means of indexing through a register file, are activated whenever a task is not executing a foreground load or store instruction. A pair of background address registers is required to provide the store and load addresses for the register context switch. The "background" store and load instructions are pre-stored context switch save and restore instructions which, when enabled, operate in the background until the save and

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restore operation has completed. Use of the eventpoint architecture is one mechanism that can be set up to test for the lack of foreground store and load instruction execution and trigger a background store and load instruction to execute. Suitable eventpoint architecture is covered in more detail in U.S. Provisional Application Serial No. 60/140,245 entitled "Methods and Apparatus for Generalized Event Detection and Action Specification in a Processor" and U.S. Application Serial No. [[_____]] 09/598,566 having the same title and filed June 21, 2000, both of which are incorporated by reference herein in their entirety. A status bit is also used to indicate the progress of the context switch so that, if preempted, it could be allowed to complete before another program context was initiated. Further details of a presently preferred register file indexing mechanism are provided in U.S. Patent Application Serial No. 09/267,570 entitled "Register File Indexing Methods and Apparatus for Providing Indirect Control of Register Addressing in a VLIW Processor" filed March 12, 1999 and incorporated by reference herein in its entirety. This register file indexing mechanism is preferably used for register file access.